

## **IDEAL POWER INC.**

Ideal Power (Nasdaq: IPWR) is the developer and provider of its innovative and widely patented B-TRAN® bidirectional semiconductor power switch. B-TRAN® offers compelling advantages over conventional technologies and addresses the demanding standards of today's solid-state circuit protection and intelligent power delivery systems. It features very low conduction losses that deliver improved power efficiency, thereby reducing energy consumption and providing cost savings. The unique bidirectional capability of B-TRAN® simplifies the design, control and diagnostics of solid-state power solutions while enabling smaller, lower cost systems. B-TRAN® delivers compelling advantages for a broad spectrum of applications including solid-state circuit breakers, static transfer switches, battery disconnect units and EV contactors that are widely used in data centers, industrial power systems, energy grid and storage systems, and electric vehicles and charging infrastructure.

## **CURRENT OPPORTUNITY**

**Position Title:** Packaging Engineer

**Job Location:** Austin, Texas

**Reports To:** Chief Operating Officer

## **POSITION SUMMARY**

Overall responsibility for packaging engineering for Ideal Power. To ensure products meet packaging and reliability requirements as well as provide feedback to drive product improvements. Candidate must be experienced with discrete semiconductor devices. Candidate must have thermal modeling experience, both for packaged devices as well as demo boards. Candidate must have excellent interpersonal, communication and interpersonal skills. Must be able to handle multiple tasks with attention to detail as well as accuracy. Ability to make timely decisions with limited information.

## **ESSENTIAL DUTIES AND RESPONSIBILITIES**

- Identify packaging solutions for new devices and design changes to existing devices.
- Assess product capabilities to fit and interact with different mold compounds, lead frame materials, CTE, solder paste in discrete packaging. Both through hole and surface mount packages.
- Identify high risk areas and participate in activities to mitigate risk, participate in developing FMEA and design for reliability activities.
- Team with QRA to ensure new device packaging is manufacturable and passes AEC-Q101 testing.

- Conformably recommending solutions for product that fails to meet qual requirements.

## QUALIFICATIONS

To perform this job successfully an individual must be a result-oriented, motivated self-starter capable of achieving goals with little guidance.

- Component characteristics and specifications (IGBT and MOSFET) and their application related to power conversion.
- Reliability statistics, modeling theory and failure mechanism in semiconductor devices and packages.
- Ability to use Altium or other packaging design software.
- Thermal modeling software experience.
- Silicon and packaging fabrication processes and materials experience and knowledge of packaging material and techniques. TO247, TO264, TOLT experience a plus.
- Wirebond and Clip interconnect experience required. AMB experience a plus.
- Reliability DOE experience.
- Failure analysis tools and technique knowledge.
- JEDEC, MLSTD-883, MILSTD-750, AECQ101, RoHs standards. Material composition report development experience.
- Must have the ability to travel to the Philippines, Taiwan, and China on periodic trips.

## EDUCATION AND EXPERIENCE

- Bachelor's degree in Mechanical Engineering, Material Science, Physics or related field. MS degree a plus.
- 10 years experience in the power semiconductor packaging.

## TRAVEL

The position is based in Austin, Texas, and modest travel will be required. The individual is expected to travel as needed, visiting major suppliers and testing facilities.

## **WORK ENVIRONMENT**

The work environment characteristics described here are representative of those an employee encounters while performing the essential functions of this job. Reasonable accommodation may be made to enable individuals with disabilities to perform the essential functions.